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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/355,961	01/30/2003	James C. Liu	10021059-1	5400

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AGILENT TECHNOLOGIES, INC.  
Intellectual Property Administration  
Legal Department, DL429  
P.O. Box 7599  
Loveland, CO 80537-0599

EXAMINER

NGUYEN, HOAI AN D

ART UNIT	PAPER NUMBER
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2858

DATE MAILED: 03/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/355,961	<b>Applicant(s)</b> LIU ET AL.	
	<b>Examiner</b> Hoai-An D. Nguyen	<b>Art Unit</b> 2858	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 January 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>01/30/2003</u> . | 6) <input type="checkbox"/> Other: ____.  |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 5, 7-10, 14, 16, 17 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Adamian (US 5,578,932).

**Adamian teaches a method and apparatus for providing and calibrating a multiport network analyzer comprising:**

- An electronic calibration device (FIG. 5, multi-state electronic transfer standard, MSETS, 14) for calibrating a network analyzer (FIG. 5, network analyzer 602) (From column 7, line 66 to column 8, line 4), with regard to claims 1, 10 and 17.
- An electronic calibration circuit (FIG. 6, microwave circuitry 25) for calibrating a network analyzer (Column 8, lines 18-19), with regard to claims 1, 10 and 17.
- A bus (FIG. 5, interface 23) (Column 8, lines 8-12), with regard to claim 10.
- A memory unit (FIG. 5, memory region 20) coupled to said bus, said memory unit comprising data characterizing a plurality of impedance states (Column 8, lines 3-12), with regard to claim 10.
- At least one port (FIG. 12, input port 170 or 172) for coupling said electronic calibration circuit to said network analyzer (Column 11, lines 45-56), with regard to claims 1, 10 and 17.

- A plurality of switching circuits (FIG. 12, switches 134, 136, 154 and 156) coupled to said port, said plurality of switching circuits operable to provide a plurality of impedance states for electronically calibrating said network analyzer (From column 16, line 60 to column 17, line 36), with regard to claims 1, 10 and 17.
- A transmission line (FIG. 12, transmission line 154) coupling at least two of said plurality of switching circuits, wherein said transmission line is short enough to reduce interactions of impedance mismatches and to reduce transmission loss (Column 16, lines 66-67), with regard to claims 1, 10 and 17.
- Said port, said plurality of switching circuits, and said transmission line are comprised within an integrated circuit (Column 16, lines 53-59), with regard to claims 1, 10 and 17.
- A processor (FIG. 5, computer control 16) coupled to said bus, said processor for electronically calibrating said network analyzer by directing said integrated circuit to provide an impedance state of said plurality of impedance states (Column 8, lines 3-17, and from column 30, line 46 to column 31, line 5), with regard to claim 10.
- Plurality of impedance states (Column 10, lines 64-66) comprises a plurality of reflective states (reflection coefficients) (Column 12, lines 14-18) and at least one transmissive state (transmission coefficients) (Column 12, lines 53-57), with regard to claims 5, 7, 14 and 19.

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- At least one resistor coupled to at least one switching circuit of said plurality of switching circuits for providing a resistive load to said switching circuit (FIG. 12, resistors connected to double throw switches 154 and 156), with regard to claims 8 and 16.
- The resistor has a resistance of 50 ohms (FIG. 12, two 50 ohms resistors connected to double throw switches 154 and 156), with regard to claim 9.

***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 2 and 11 rejected under 35 U.S.C. 103(a) as being unpatentable over Adamian in view of Heuermann (US 6,008,656).

**Adamian teaches all that is claimed as discussed in the above rejection of claims 1, 5, 7-10, 14, 16, 17, and 19, but he does not specifically teach the following:**

- The electronic calibration device/circuit is operable for calibrating said network analyzer at a high frequency.

**However, Heuermann teaches an arrangement for calibrating a network analyzer for on-wafer measurement at integrated microwave circuits comprising:**

- The electronic calibration device/circuit is operable for calibrating said network analyzer at a high frequency (Column 5, lines 32-41), with regard to claims 2 and 11.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method and apparatus for providing and calibrating a multiport network analyzer of Adamian to incorporate the teaching of an arrangement for calibrating a network analyzer for on-wafer measurement at integrated microwave circuits taught by Heuermann since Heuermann teaches that such an arrangement is beneficial to form a space between the calibration standards portion and the metallic base plate large enough so that the considerable measurement errors occurring especially at higher frequencies in the GHz range or influences of the metallic base plate on the calibration standards portion giving rise to high-frequency dependent micro-stripline fields during calibration measurement are avoided as disclosed in column 5, lines 32-41.

3. Claims 3, 12 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adamian in view of Senda et al. (JP 09115708).

**Adamian teaches all that is claimed as discussed in the above rejection of claims 1, 5, 7-10, 14, 16, 17, and 19, but he does not specifically teach the following:**

- The integrated circuit has a package size small enough to avoid cavity resonance at a high frequency.

**However, Senda et al. teaches an electromagnetic wave absorbing material and package comprising:**

- The integrated circuit has a package size small enough to avoid cavity resonance at a high frequency (SOLUTION paragraph), with regard to claims 3, 12 and 18.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method and apparatus for providing and calibrating a

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multiport network analyzer of Adamian to incorporate the teaching of an electromagnetic wave absorbing material and package taught by Senda et al. since Senda et al. teaches that such an arrangement is beneficial to provide an electromagnetic wave absorbing material which shows an electromagnetic wave absorbing effect even at such a high frequency as several tens of GHz and a package which can suppress cavity resonance even at such a high frequency as several tens of GHz can be obtained as disclosed in the SOLUTION paragraph.

4. Claims 4 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adamian in view of Heuermann as applied to claims 2 and 11 above, and further in view of Vandersteen et al. (US 2002/0003455).

**Adamian and Heuermann teach all that is claimed as discussed in the above rejection of claims 2 and 11, but they does not specifically teach the following:**

- The high frequency is a frequency greater than 26.5 gigahertz.

**However, Vandersteen et al. teaches a broadband high frequency differential coupler comprising:**

- A HP8510C calibrated network analysers operable from 45 MHz up to 50 GHz  
(Page 6, paragraph [0129]), with regard to claims 4 and 13.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method and apparatus for providing and calibrating a multiport network analyzer of Adamian to incorporate the teaching of using a HP8510C calibrated network analysers operable from 45 MHz up to 50 GHz taught by Vandersteen et al. since Vandersteen et al. teaches that such an arrangement is beneficial to deal with high frequency signals above 5 GHz as disclosed in Page 6, paragraph [0129].

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5. Claims 6, 15 and 20 rejected under 35 U.S.C. 103(a) as being unpatentable over Adamian in view of Oldfield et al. (US 5,587,934).

**Adamian teaches all that is claimed as discussed in the above rejection of claims 1, 5, 7-10, 14, 16, 17, and 19, but he does not specifically teach the following:**

- The plurality of reflective states comprises at least one low reflective state.

**However, Oldfield et al. teaches an automatic VNA calibration apparatus comprising:**

- The plurality of reflective states comprises at least one low reflective state (Column 4, lines 65-67), with regard to claims 6, 15 and 20.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method and apparatus for providing and calibrating a multiport network analyzer of Adamian to incorporate the teaching of an arrangement for calibrating a network analyzer for on-wafer measurement at integrated microwave circuits taught by Oldfield et al. since Oldfield et al. teaches that such an arrangement is beneficial to provide a low loss, low reflective through-connection between the test ports as disclosed in column 2, lines 5-7.

### ***Conclusion***

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant's attention is invited to the followings whose inventions disclose similar devices.

- Bockelman et al. (US 5,793,213) teaches a method and apparatus for calibrating a network analyzer.



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- Dunsmore (US 6,643,597) teaches calibrating a test system using unknown standards.

### CONTACT INFORMATION

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoai-An D. Nguyen whose telephone number is 571-272-2170. The examiner can normally be reached on M-F (8:00 - 5:30) First Friday Off.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, N. Le can be reached on 571-272-2233. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HADN

Hoai-An D. Nguyen  
Examiner  
Art Unit 2858

HADN

  
JAY PATIDAR  
PRIMARY EXAMINER